Method and Apparatus for Multi-Port Memory Controller

ABSTRACT OF THE DISCLOSURE

A memory controller is provided. The memory controller includes an initiator block configured to arbitrate requests corresponding to data from multiple ports. The initiator block includes an arbitration module configured to consider a latency factor and a bandwidth factor associated with the data from a port to be selected for processing. A state machine is in communication with the arbitration module. The state machine is configured to generate a signal to the arbitration module that is configured to select the data associated with the port based upon the latency factor and the bandwidth factor. Task status and completion circuitry configured to calculate the bandwidth factor based upon previous data selected from the port is included in the initiator block. The task status and completion circuitry is further configured to transmit the calculated bandwidth factor to the state machine. A method for arbitrating across multiple ports is also provided.